BUS ARBITRATOR SUPPORTING MULTIPLE ISOCHRONOUS STREAMS IN A SPLIT TRANSACTIONAL UNIDIRECTIONAL BUS ARCHITECTURE AND METHOD OF OPERATION

ABSTRACT OF THE DISCLOSURE

There is disclosed a bus interface unit for transferring data between a plurality of bus devices. The bus interface unit comprises: 1) a first bus device interface comprising: a) a first incoming request bus for receiving request packets from a first one of the plurality of bus devices; b) a first outgoing request bus for transmitting request packets to the first bus device; c) a first incoming data bus for receiving data packets from the first bus device; and d) a first outgoing data bus for transmitting data packets to the first bus device; 2) a second bus device interface comprising: a) a second incoming request bus for receiving request packets from a second one of the plurality of bus devices; b) a second outgoing request bus for transmitting request packets to the second bus device; c) a second incoming data bus for receiving data packets from the second bus device; and d) a second outgoing data bus for transmitting data packets to the second bus device; and 3) an arbitration circuit for determining a first priority level associated with a first request packet received from the first bus device and determining a second priority level associated with a

second request packet received from the second bus device.